CLAIMS

1. A method comprising:

creating mappings from a logical address space to physical memory;

identifying portions of the logical address space based on usage;

modifying the mappings to reduce the number of physical memory devices that are targeted by the mappings; and

receiving memory instructions that reference memory in terms of the logical address space.

2. A method as recited claim 1, wherein the mappings comprise mappings from one or more virtual address spaces to a physical address space.

3. A memory controller comprising:

means for receiving memory instructions that reference memory in terms of a logical address space;

means for identifying portions of the logical address space based on usage; and

means for mapping the identified portions of the logical address space to physical memory in a manner that reduces the number of physical memory devices referenced by the identified portions of the logical address space.

4. A memory controller as recited in claim 3, wherein the means for identifying include means for monitoring the memory instructions to determine more frequently used portions of the logical address space.

5. A memory controller as recited in claim 3, wherein the means for identifying include means for monitoring the memory instructions to determine more recently used portions of the logical address space.

6. A memory controller as recited in claim 3, wherein the means for identifying include means for receiving notifications regarding logical memory allocations and de-allocations.

7. A memory controller as recited in claim 3, wherein the means for identifying include means for receiving notifications regarding actual usage of logical memory addresses.

8. A memory controller as recited in claim 3, wherein the means for identifying action include means for maintaining one or more in-use registers indicating whether corresponding portions physical memory are currently in use.

9. A memory controller as recited in claim 3, further comprising:

means for identifying one or more memory devices that are not referenced by the identified portions of the logical address space; and

means for setting said one or more identified memory devices to a reduced power mode.

10. A memory controller as recited in claim 3, wherein the means for identifying includes means for monitoring the memory instructions to determine more frequently used portions of the logical address space, the memory controller further comprising:

means for identifying one or more memory devices that are not referenced by the identified portions of the logical address space; and

means for setting said one or more identified memory devices to a reduced power mode.

11. A memory controller as recited in claim 3, wherein the means for identifying includes means for monitoring the memory instructions to determine more recently used portions of the logical address space, the memory controller further comprising:

means for identifying one or more memory devices that are not referenced by the identified portions of the logical address space; and

means for setting said one or more identified memory devices to a reduced power mode.

12. A memory controller as recited in claim 3, further comprising:

means for identifying one or more physical memory areas that are referenced by the identified portions of the logical address space; and

means for setting said one or more physical memory areas to a reduced power mode.

13. A memory controller as recited in claim 3, wherein the means for identifying includes means for monitoring the memory instructions to determine more frequently used portions of the logical address space, the memory controller further comprising:

means for identifying one or more physical memory areas that are not referenced by the identified portions of the logical address space; and

means for setting said one or more physical memory areas to a reduced power mode.

14. A memory controller as recited in claim 3, wherein the means for identifying includes means for monitoring the memory instructions to determine more recently used portions of the logical address space, the memory controller further comprising:

means for identifying one or more physical memory areas that are not referenced by the identified portions of the logical address space; and

means for setting said one or more physical memory areas to a reduced power mode.

15. A memory controller as recited in claim 3, further comprising means for periodically repeating the identifying and mapping actions to repeatedly reduce the number of physical memory devices referenced by the identified portions of the logical address space.

16. A memory controller as recited in claim 3, further comprising:

means for periodically repeating the identifying and mapping actions to repeatedly reduce the number of physical memory devices referenced by the identified portions of the logical address space; and

means for moving affected portions of physical memory so that each logical address continues to reference the same data prior to any repeated mapping action.

17. A method of managing memory, comprising:

monitoring memory accesses to identify portions of a logical address space based on usage; and

periodically re-mapping the logical address space to physical memory to reduce the number of physical memory devices referenced by the identified portions of the logical address space.

18. A method as recited in claim 17, wherein the monitoring comprises monitoring the memory instructions to determine more frequently used portions of the logical address space.

19. A method as recited in claim 17, further wherein the monitoring comprises monitoring the memory instructions to determine more recently used portions of the logical address space.

20. A method as recited in claim 17, further comprising:

receiving memory instructions that reference memory in terms of the logical address space; and

monitoring the memory instructions to identify the portions of the logical address space.

21. A method as recited in claim 17, wherein the identified portions of the logical address space are those portions that are used least frequently, further comprising:

identifying one or more memory devices that are not referenced by the identified portions of the logical address space; and

setting said one or more identified memory devices to a reduced power mode.

22. A method as recited in claim 17, wherein the identified portions of the logical address space are those portions that are used least recently, further comprising:

identifying one or more memory devices that are not referenced by the identified portions of the logical address space; and

setting said one or more identified memory devices to a reduced power mode.

23. A method as recited in claim 17, wherein the identified portions of the logical address space are those portions that are used least frequently, further comprising:

identifying one or more physical memory areas that are not referenced by the identified portions of the logical address space; and

setting said one or more physical memory areas to a reduced power mode.

24. A method as recited in claim 17, wherein the identified portions of the logical address space are those portions that are used least recently, further comprising:

identifying one or more physical memory areas that are not referenced by the identified portions of the logical address space; and

setting said one or more physical memory areas to a reduced power mode.

25. A method as recited in claim 17, further comprising:

prior to any re-mapping action, moving affected portions of physical memory so that each logical address continues to reference the same data.

26. A system comprising:

a plurality of physical memory devices containing physical memory;

a memory controller configured to reference the physical memory in response to received memory instructions specifying addresses in terms of a logical address space;

an operating system configured to dynamically allocate memory from the logical address space and to identify allocated portions of the logical address space to the memory controller;

wherein the memory controller is configured to respond to the operating system by mapping allocated portions of the logical address space to corresponding portions of physical memory in a manner that tends to reduce the number of physical memory devices referenced by the allocated portions of the logical address space.

27. A system as recited in claim 26, wherein:

the operating system is further configured to dynamically de-allocate memory from the logical address space and to identify the de-allocated portions of the logical address space to the memory controller; and

the memory controller is further configured to respond to identifications of de-allocated portions of the logical address space by re-mapping currently allocated portions of logical memory to reduce the number of physical memory devices referenced by allocated portions of logical memory.

28. A system as recited in claim 26, wherein the memory controller is configured to maintain one or more in-use registers indicating which portions of physical memory are currently in use.

29. A memory management system comprising:

means for maintaining a free region list indicating free memory regions for potential allocation from physical memory devices;

means for sorting the free region list in an order that is based on the relative current allocations of memory regions from respective sets of one or more physical memory devices; and

means for allocating memory regions indicated by the sorted free region list on the sorted order so that the memory regions are allocated preferentially from those physical memory devices having higher relative current allocations of memory regions.

30. A memory management system as recited in claim 29, further comprising:

means for identifying one or more memory devices having relatively lower current allocations of memory regions; and

means for setting said one or more identified physical memory devices to a reduced power mode.

31. A memory management system as recited in claim 29, further comprising means for maintaining the free region list as a linked list of free region indicators.

32. A memory management system as recited in claim 29, further comprising means for repeatedly re-sorting the free region list in said order.